A frequency multiplier.

TECHNICAL FIELD

5   The present invention relates to a device for multiplying the frequency of a signal in the form of a pulse train, the device comprising input means for the signal and a plurality of access means for accessing the signal at points with a predetermined phase difference between said points.

10   BACKGROUND ART

Frequency multipliers are important building blocks in a variety of technologies, for example communication systems. A wide range of frequencies is often desired, thus creating a desire for tuneable frequency multipliers. In general, the noise characteristics of frequency multipliers get

15   worse the wider the tuning range of the generator. Thus, trade-offs have to be made with contemporary frequency multipliers regarding tuning range and noise characteristics. In order to live up to noise specifications, it may thus be necessary to use a plurality of different frequency multipliers to cover a wide frequency band.

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The present invention is directed mainly to the field of digital frequency multipliers, and thus, to solve the problems of that category of frequency multipliers. Among those problems, the following could be mentioned:

25   Usually, only multiplication factors in the form of 2^n, where n is an integer, can be obtained. In solutions where factors other than 2^n can be obtained, a fixed width pulse is clocked in different integer values of the minimum pulse width. This results in an output frequency spectrum rich in unwanted frequency components. It also adds asymmetry and circuit complexity not

30   suitable for higher frequencies, such as the microwave range.

Also, many suggested digital multipliers are asymmetrical with respect to the different signals, which is particularly troublesome at very high frequencies.

5   Many solutions are also quite complex, and add jitter. In addition, many digital multipliers use logic circuits such as XOR or OR gates to generate pulses both on rise and fall. This may result in varying curve forms in consecutive pulses in the output of the multiplier.

10 It should be pointed out that the phrase "frequency multiplier" in this text refers to the pulse frequency in a pulse train.

DISCLOSURE OF THE INVENTION

In order to overcome the problems of contemporary digital frequency multipliers, the present invention proposes a device for multiplying the pulse
15 frequency of a signal in the form of a pulse train, the device comprising input means for the signal and a plurality of access means for accessing the signal at points with a predetermined phase difference between said points.

The device additionally comprises a plurality of means at a first level for
20 combining accessed signal pairs, there being one and the same phase distance within all the combined pairs, where the output from each first level combining means is a new pulse train.

The device also comprises combining means at a second level for combining
25 the pulse trains from the first level into one single pulse train, and according to the invention, the combining means at the first level are such that the pulses in their output pulse trains have rise flanks which always coincide with the rise flank from the first signal in the combined accessed signal pairs, and fall flanks which always coincide with the fall flanks of the second signal in
30 said pair.

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The advantages of this design will become evident in the following detailed description.

Suitably, the phase distance within the combined signal pairs are calculated according to the formula (360/[2*N]) + 180, where N is the desired multiplication factor, N being any number, integer or non-integer, greater than 1.

Saying that a first signal is delayed by 360/([2*N])+180 with respect to a second signal is also equivalent to saying that the second signal is delayed by 360-(360/([2*N])+180)=180-(180/N) with respect to the first signal, since a phase difference of 360° is indistinguishable from a phase difference of 0°.

Also, since the first level combining means do not make any distinction between the first and the second signal in each pair, a positive and a negative phase difference of the same absolute value are equivalent.

Preferably, the combining means at the first level comprise logic circuits with an AND-function, and the combining means at the second level comprise logic circuits with an OR-function.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be describe in more detail in the following, with reference to the appended drawings, in which

Fig 1 shows an embodiment of the invention which provides multiplication by four, and

Fig 2 shows a first combination of signals according to the invention,

Fig 3 shows an embodiment of the invention with variable multiplication factor, and

Fig 4 shows a switch suitable for use in the embodiment of fig 2, and

Fig 5 shows an embodiment of the invention which enables multiplication by non-integer factors, and

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Fig 6 and 7 show a component for use in the non-integer multiplier, and Fig 8 shows a delay component for use in the invention.

EMBODIMENTS

5   In fig 1, a first embodiment of a device 100 according to the invention is shown:

An input signal, a pulse train with a basic pulse frequency f_{in}, is input to the input port 110 of the device. The input port inputs the signal to a component

10   120, preferably a delay line, which can be "tapped" or accessed at various intervals so that a plurality of signal "pairs" with equal phase separation within each pair can be obtained.

The phrase "phase separation within the pairs" refers to the fact that each

15   pair contains a first and a second signal sample, with a phase distance between them.

A pulse train with a pulse frequency four times higher than the input pulse frequency f_{in} is obtained by the device 100 in the following manner:

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The phase difference within each pair is, according to the invention, calculated according to the equation **(360/[2*N] + 180)**, where N is the desired multiplication factor. As will be shown later on, N can be virtually any number, integer or non-integer, greater than 1. Thus, in the case of a

25   "multiply by four" device as in fig 1, the phase difference should be 360/8 + 180 = 225 degrees, or equivalently 180-(180/N)=180-(180/8)=135

This is also the design of the device in fig 1, with the input signal being accessed at the following eight points, and pairwise input to four combining

30   devices A, B, C, D:

- A: 45 – 270   = 225

- B: 135 – 360   = 225
- C: 90 – 225   = -135
- D: 180 – 315   = - 135

5   It should be pointed out here that the phase difference in the last two pairs above, i.e. -135 degrees, fulfils the condition of the equation, since adding 360° does not change the phase difference and 360° + (−135°) = 225°.

Turning now to fig 2, the combinatorial principle of the device in fig 1 will be
10   shown: At the top of the figure, two pulse trains are shown, with a phase difference of 225 degrees between them, as in the pairs in the example shown in fig 1. Below the two pulse trains, there is shown a pulse train which is formed as the output from the combining devices shown in fig 1 and being comprised in the invention, the combining device having the function of an
15   AND-gate or a circuit with a similar function, e.g. a NAND-gate and an inverter.

As can be seen from fig 2, the pulse train which results from the combination is a pulse train with the same pulse frequency as the input pulse train to the
20   device, but with reduced pulse width.

Another interesting feature of the invention will also become apparent when studying the diagrams of fig 2: since both of the combined signals are pulse trains (actually one and the same pulse train accessed at points with different
25   phases), both signals comprise pulses, with the pulses having a "rise" flank and a "fall" flank. The signal which results as a combination of the two signals is also a pulse train, with the pulses having rise and fall flanks. The feature to be noted is that the rise flanks of the pulses in the combined signal all coincide with rise flanks in pulses in one and the same of the combined
30   signals, as is also the case with the fall flanks of the pulses in the combined signal. This is beneficial due to the fact that all of the pulses in the combined

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signal will have identical shapes, since they are all created from identical pulse shapes (rise/fall).

In the example shown in fig 2, the rise flanks of the combined signal coincide
5   with the rise flanks of the signal shown at the top , i.e. the signal with "phase zero", and the fall flanks of the combined signal coincide with the fall flanks of the second signal, i.e. the signal that is 225 degrees delayed with respect to "the zero signal".

10   Reverting now to fig 1, it is shown in this fig that the output signals from combining means are used as input to a second combining means E. Thus, the AND-function can be seen as a first level combination of signal pairs, the device also comprising a second level combination for the output signals from the first level combination.
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The second level combination device E is a circuit with the function of an OR-gate or an XOR-gate, and the resulting output signal is shown in fig 3: In this fig, the output signal from each of the four first level combiners are shown, labelled A-D, and it will become apparent that these four pulse trains all have
20   the same pulse frequency, but with the pulses appearing at different times, so that they may readily be combined into one pulse train, shown at the bottom of fig 3.

Naturally, the combination of four pulse trains, each with the same pulse
25   frequency f_{in} as the input pulse train, will result in a pulse train with four times that frequency, i.e. $4 * f_{in}$, which was the purpose of the device shown in fig 1. Thus, a "times four"- frequency multiplier has been obtained.

An observation can be made here regarding the phase difference between
30   the pulse pairs which are combined at the first level: the phase difference should be chosen so that the signals generated by the first level combining means become "equidistant" within 360 degrees, i.e. if four combiners are

used, the phase difference should be 360/4=90. With reference to fig 1, it can be seen that the first signals are indeed 45, 135, 225, 315, thus ninety degrees between each of the first signals.

5   Once these phases and their order have been fixed, it is important that the second of the signals in each signal pair are shifted by the same amount in all pairs, i.e. +225° (=-135°) in all cases OR +135° (=-225°) in all cases.

In fig 4, another embodiment 400 of the present invention is shown: the
10   embodiment of fig 4 serves to illustrate that the multiplier according to the present invention may be used to achieve variable multiplication factors. Thus, the multiplier of fig 4 resembles the multiplier shown and described with reference to figs 1-3, in that it also comprises a delay line 420 which can be accessed at multiple points with a chosen phase distance between said
15   points.

The accessed signal is then fed pairwise to first level combining circuits, A', B', C', D' as with the previous embodiment, there being one and the same phase distance between the first and the second signals in the pairs, and
20   also with one and the same phase distance between consecutive first signals in each pair.

In addition to the earlier embodiment, the device shown in fig 4 also comprises a set of switches, so that the second signal in each pair can be
25   accessed from alternate points in the delay line, thus creating the possibility of altering the phase difference between the first and the second signals that are combined into pairs.

Bearing in mind the expression shown previously, i.e. **(360/[2*N] + 180)** or
30   **(180–180/N),** where N is the desired multiplication factor, it can thus be seen how the switches shown in fig 4 may be employed to alter the multiplication factor. If the positions shown in fig 4 are maintained, a "times two"- multiplier

will be obtained. Reverting to the equation, a "times two"—multiplier should have a phase difference of 360/4 + 180 = 270, which is true of the circuit on fig 4 with the switches in the positions shown in the figure.

5   Thus, instead of the signal pairs shown previously, the following signal pairs will be obtained, the combiners being referred to from left to right in fig 4:

Combiner	First signal phase	Second signal phase
A	45	315
B	Not used due to switch position	
C	225	135
D	Not used due to switch position	

As can be seen, the phase differences are 45–315 = -270, and 225-135 = 90 = -270.

However, if the switches are flipped, the phase distance within the pairs will instead be as follows:

Combiner	First signal phase	Second signal phase
A	45	270
B	135	360
C	225	90
D	315	180

Thus, by flipping the switches, two additional combiners are enabled, resulting in four output signals (A, B, C, D), each with a phase distance between their respective first and second signals of:

A: -225

B: -225

C: 135

D: 135

As previously, -225° can be considered as equivalent to -225°+360°=135°.

Accordingly, a "multiply by four" circuit is obtained by flipping the switches to
5   the alternate position. As with the previous embodiment in fig 1, the output
pulse trains from the first level combiners are then combined by means of an
OR-circuit or an XOR-circuit, E'

As will be realised from looking at the circuit in fig 4, some of the switches (45
10   and 225 degrees) are shown for reasons of symmetry only, and should never
be switched.

The switches can be implemented in any of a number of well known and
suitable ways, and will not be elaborated upon in depth here. However, for
15   the sake of clarity, one possible switch embodiment 500 is shown in fig 5, a
so called transmission gate switch. As shown in fig 5, this kind of switch
comprises a parallel connection of a PMOS-transistor and an NMOS-
transistor. This kind of switch offers a symmetrical transfer function with
respect to a control voltage used for operating the switch, and provides a low
20   ON resistance and a high OFF impedance. Since switches are used, no
noise or jitter is added by the device of fig 4.

The general principle behind the multiplier of the present invention will have
been realized by now. However, by way of example, it could be pointed out
25   that a "multiply by three" circuit could be achieved by accessing a delay line
at   points   where   the   signal   has   respective   phase   positions   of
60°, 120°, 180°, 240°, 300° and 360°.

Using AND-circuitry, the signals are then paired as follows: 300°–60°, 60°-
30   180°, 180°–300°, thus fulfilling the basic condition of (360/[2*N] + 180), N in
this case being three, thus 360/6 + 180 = 60 +180 =240. These pairs are
then combined in an OR-circuit as shown in figs 1 or 4.

If the delay is split into 24 equidistant phases, the multiplier can, for example by means of switches, be set to any of the multiplication factors 2, 3, 4, 6 or 12 by properly applying the principle behind the invention when combining the phases. The principle can be applied to any multiplication factor >1, including non-integer factors, an example of which will be shown below, in connection to fig 6.

In fig 6, a non-integer multiplier 600 using the present invention is shown. In the device of fig 6, a "multiply-by-1.5"–circuit is obtained by combining the phases such that 3 periods of the accessed signal is realized for 2 periods of the input signal.

Suitably, the input signal is accessed at delays of up to two periods, and the accessed signal is combined pairwise using three AND-type circuits A", B", C".

As with the previously described multipliers, the multiplier 600 in fig 6 utilizes first level combiners, in this case AND-gates. The device 600 uses three AND-gates as first level combiners, in which the accessed input signal is combined pairwise in the following fashion:

- 360° - 60°
- 600° - 300°
- 120° - 540°

As can be seen, the principle of **(360/[2*N] + 180),** N being the desired multiplication factor is adhered to, since 360/2*1.5 + 180 = 300. (120-540 = - 420 = 2*360 – 420 = 300)

From the AND-gates, pulses of the correct width for multiplication by 1.5 are produced. However, one pulse is output from each AND-gate for each period of the input signal, thus producing twice as many pulses as desired.

5   To avoid having multiple pulses, two in this case, coming from a single AND-type circuit during the two periods of the input signal, the outputs from the AND-gates are gated by flip-flops before being output to the OR-gate. These flip-flops transfer the signal from D to Q only if Enable has been engaged (the signal will be transferred all the time until Reset is given, even if Enable goes

10   low again). If Reset is engaged, the Q output is reset to zero and kept there until next Enable pulse is given. The Enable and Reset signals are provided by the Q output of the previous and next pulses in the pulse train respectively.

15   The outputs from the flip-flops are input to an OR-gate E" which combines the individual pulse trains from the AND-gates into a single pulse train with a pulse frequency which is 1.5 that of the pulse train input to the device.

During start-up of the device 600, or when, for example, changing

20   multiplication factor, all flip-flops but one (e.g. the first) have to be given a reset signal to ensure stable operation. This can be provided by placing an additional OR-gate at the Reset input of all flip-flops but the first. One of the inputs to the OR-gate is as in Fig 6, the other is the "start-up" reset signal. On the first flip-flop an extra OR-gate is placed at the Enable input where the

25   "start-up" reset signal is given as one input making sure that the first flip-flop is open at "start-up".

An example of how a gated flip-flop for use in the device 600 can be implemented is shown in fig 7. It comprises an SR-type flip-flop, which has a

30   truth table shown in fig 8, and a switch.

If Enable is high, or Enable is the last SR flip–flop input that was high, the output of the SR flip-flop is high. When the S R flip-flop output is high the switch is closed and the input of the device 60O, Q, is passed to the device 600 output. When Reset goes high, the output of the SR flip-flop goes low

5   and stays low until Enable goes high again. When the SR flip-flop output goes low, the switch goes into the position where the device 600 output is grounded (goes low).

However, a two period delay as shown in fig 6 is not always required. For

10   example, the 600° input can be replaced by the 600-360=240° input, as long as the sequence of Enable-Reset signals is retained. In certain cases, it could still be preferable to have a two period delay, e.g. if sequential input pulses are not identical like in a frequency modulated signal.

15   In addition, any 1/2 multiplication factor >1, i.e. 1.5, 2.5, 3.5 etc., can be achieved by proper choice of output phases utilizing a delay of two input periods, or a two period sequence of a single period delay. For a 3 period delay, or a three period sequence of a single period delay, any 1/3 multiplication factor >1, i.e. 1.33, 1.67, 2.33, 2.67 etc., can be achieved in a

20   similar manner. For an n period delay, or an n period sequence of a single period delay, any N+M/n, where N and M are integer numbers ≥1, multiplication factor and be achieved.

The n-period delay used in some embodiments of the invention can, for

25   example be designed with the use of *n* so called Delay Locked Loops connected in series. An example of a suitable DLL is shown in fig 9. Since DLL:s as such are previously known, they will not be described in further depth here.

30   In addition, the delay could also be realized by comparing the phase at the output of the second delay directly with the input phase of the first delay. The delay itself could, apart from DLL:s, be of any kind, e.g. active circuits

(inverters) or tunable passive delay lines. Another type of delay which could be used is a ferroelectric tunable delay line.

Thus, as has been shown by means of the embodiments of the invention shown above and in the appended drawings, with the proper choice of oscillator tuning range and devices with controllable multiplication factors according to the invention, very wide range frequency generators can be realized.

As an example, consider a VCO with an operation frequency range of f_0 to f_1. Further assume that $f_1 = 1.4f_0$. If a multiplier with variable multiplication factors of 1.3, 1.5, 2, 2.5, 3 and 4 are connected to the VCO, the entire frequency range between f_0 and $4f_1 = 5.6f_0$ will be covered.

In conclusion, the invention offers the possibility of frequency multipliers with, for example, the following advantages:

- The use of AND (or NAND) gates makes the waveform more symmetrical.
- Integer multiplication factors other than 2^n can be achieved with low content of other frequency components
- Non-integer multiplication factors can be achieved with low content of other frequency components
- The multiplication factor can be varied by a control signal (i.e. controlling switches as shown in fig 4).
- The signal paths can be made symmetrical.
- Subsequent pulses have identical waveforms since they are generated from identical pulse "edges"
- A system with one VCO and a controllable multiplier makes a very compact, flexible, wide band, general purpose frequency generator, which would be straight forward to integrate on a single chip.